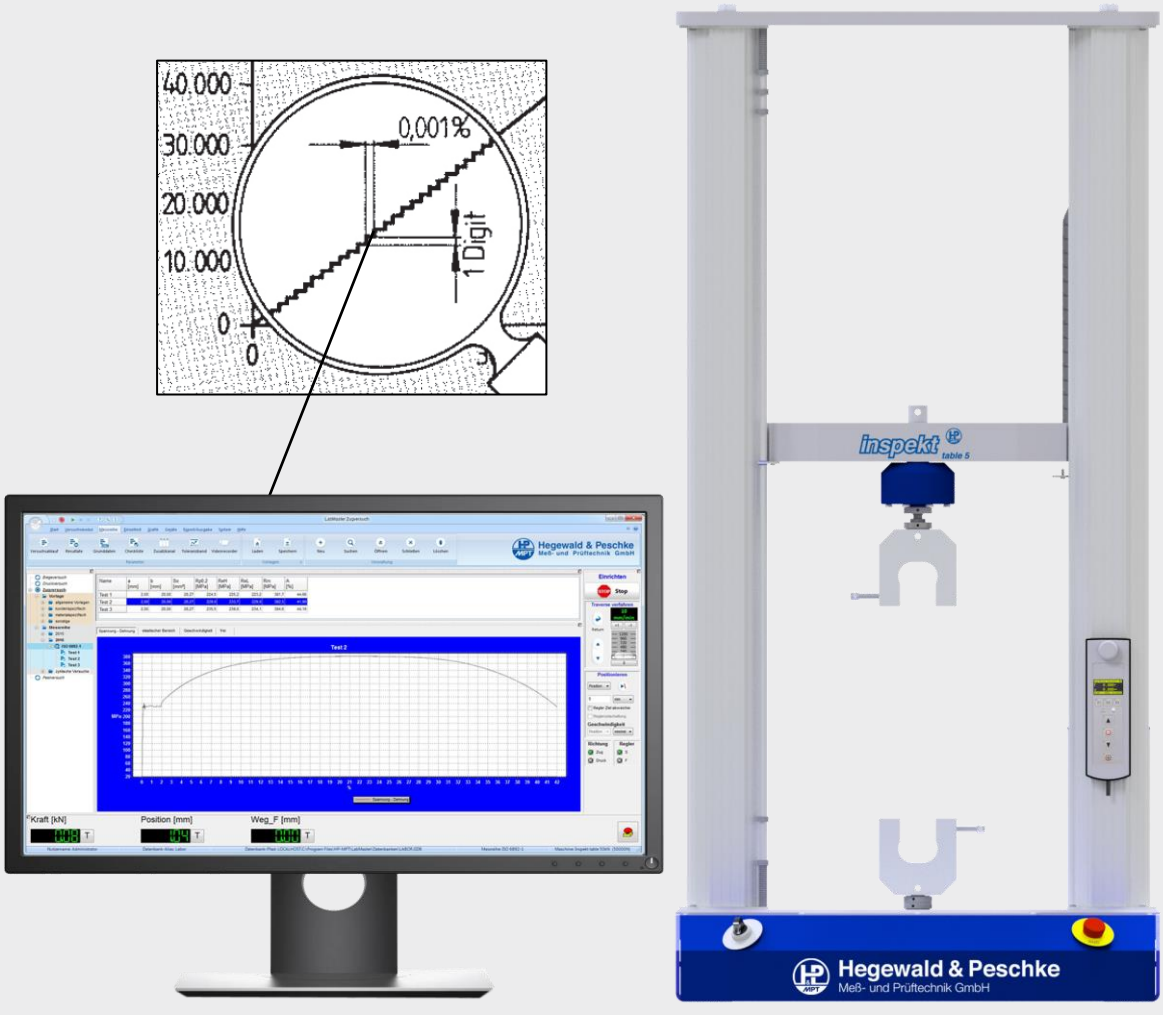
Hegewald & Peschke
Meß- und Prüftechnik GmbH

Load measurement in Universal Testing Machines

From load cell to the displayed measuring channel.



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A. How does a force transducer work?

A.1 Load cell based on strain gauges

The measurement is based on the elastic deformation of a spring body. Applying a force causes an elastic deformation of this spring body. This stretching or compression is determined by means of applied strain gauges.

From physics, the concept of a Wheatstone's bridge circuit is known for the determination of ohmic resistances. This principle is also used in load cells.

The relative change in resistance is proportionally dependent on the strain/ compression.

The output signal of the bridge circuit therefore provides information about the deformation.

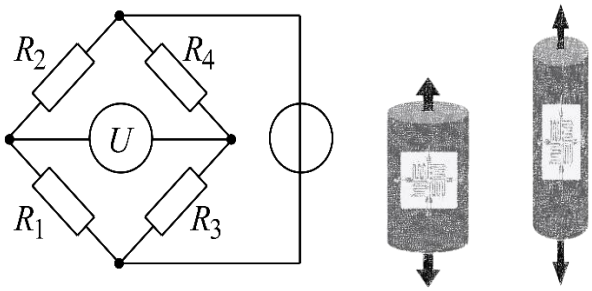
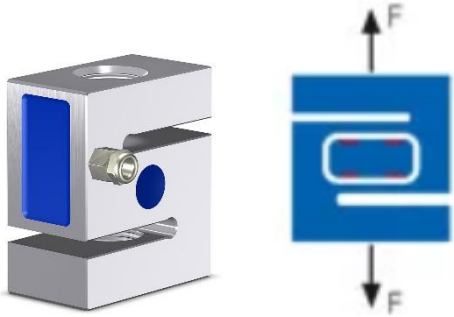


Fig. 1: Wheatstone's bridge

Since the force is also proportional to the stretching/compression, this can be determined linearly from the determined change in resistance on the basis of a calibration.

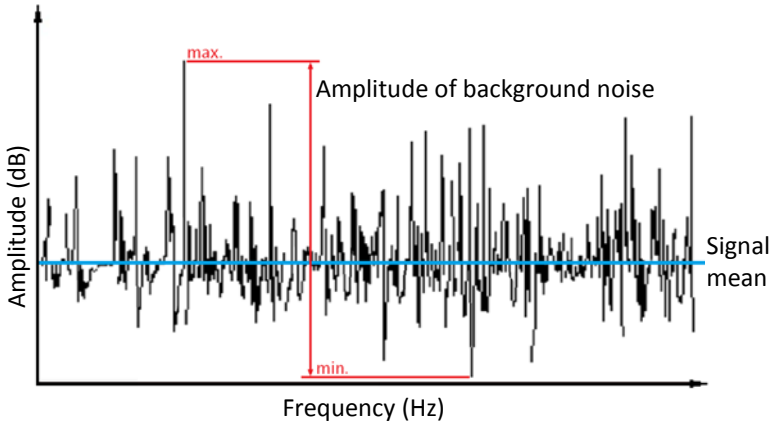
Depending on the arrangement of the strain gauges and the design of the load cell, a basic distinction is made between S- or Z-type load cells and ring or abbreviated R-type load cells. (S, Z- and R-type load cell). Depending on their design, the cells differ regarding overload and lateral force resistance.

R type design	S/Z type design
	
Fig. 2: R type load cell	Fig. 3: S/Z type load cell

B. The concepts of resolution and noise

B1. Resolution according to DIN EN ISO 7500-1:2018

The resolution of a measurement is defined by the sum of the theoretical resolution of the display device and half the span of the measurement signal fluctuation that occurs when the test device is switched on and the force measuring unit is unloaded (taking into account any electrical noise). The accuracy of the control of a machine, for example of hydraulic machines, is not included and must be considered specifically depending on the application.



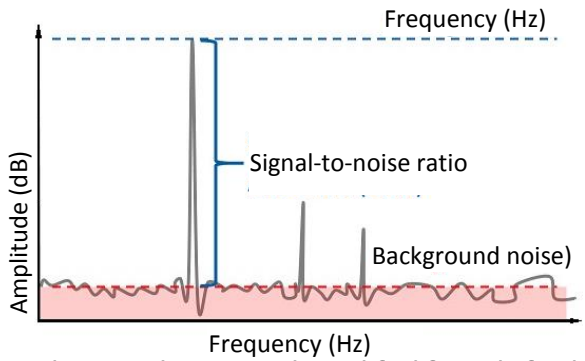
Resolution =

Theoretical resolution
+
Half amplitude of background noise

Fig. 4: Schematic diagram of background noise and simplified formula for determination of the measurement resolution

B2. Noise

Where signals are detected, there is always some background noise. The task of circuit and signal technology is to achieve the best possible approximation to the limits set by nature with regard to noise minimisation. The **signal-to-noise ratio (SNR)** is a measure of the technical quality of a useful signal that is overlaid by a noise signal.



$$SNR\ [dB] = \frac{Desired\ signal}{Background\ noise}$$

Fig. 5: Schematic diagram and simplified formula for determination of the signal-to-noise ratio (SNR)

In order to be able to extract information reliably from the signal, the useful signal must stand out clearly from the background noise, i.e., the SNR must be sufficiently large.

C. Measurement chain

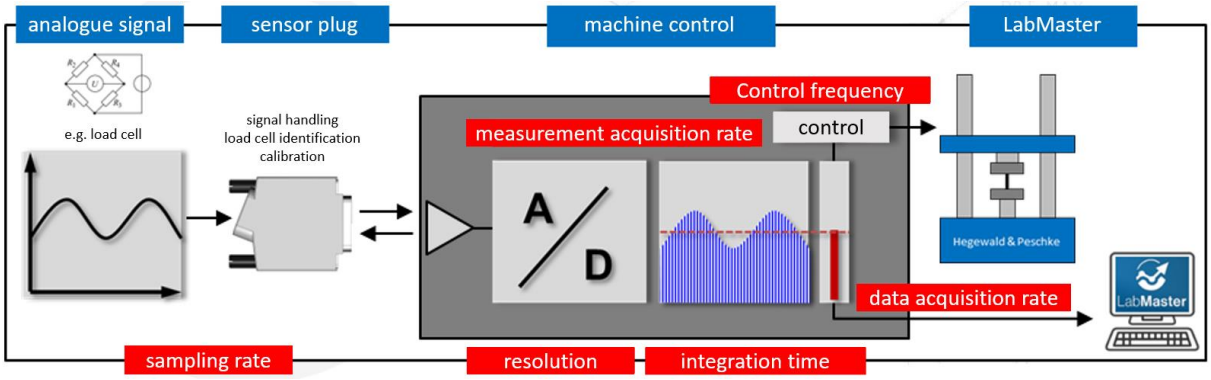


Fig. 6: Process of data acquisition in a Universal Testing Machine: from incoming analogue signal to the processed, digital signal

Term	Explanation
Sampling rate	Frequency with which the measuring amplifier scans the sensor.
Measurement acquisition rate	Frequency for transmission of measurement data from amplifier to control.
Control frequency	Internal rate for control in the EDC.
Resolution	Value that indicates how accurately a measured value can be digitally displayed.
Integration time	Time interval in which a moving average takes place over the recorded measured values.
Data acquisition rate	Frequency for data transmission from control to LabMaster.
EEPROM	Electrically Erasable Programmable Read-Only Memory: Memory (e.g. for capacity and calibration) which can be deleted/updated
A/D	Analogue digital converter (see paragraph D)

⇨ CONCLUSION: To assess the **quality of the force measurement**, the **entire measurement chain** must be taken into account. This begins with the force transducer, the transfer and processing of the analogue signal in the A/D converter and the transfer of the **measuring channel** to the test PC or as a **control variable** to the testing machine.

⇨ Consequently, the **control precision** depends on the one hand on the **force measuring chain** AND on the other hand on the **design of the testing machine drive**. This means that a backlash-free transmission from the motor via the gearbox to the spindles for moving the moving crosshead is necessary.

D. The analogue-to-digital converter (A/D converter)

D1. Principle of an analogue-to-digital converter

The main purpose of an A/D converter is to convert conditioned analogue signals (KMZ) into a stream of digital data that can be processed for display, storage and analysis through a defined form of sampling.

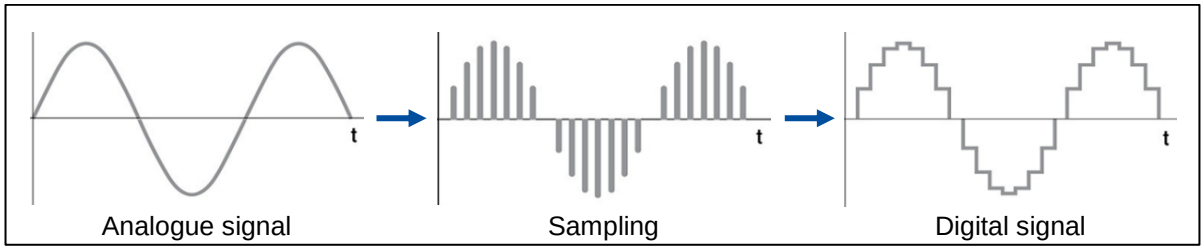


Fig. 7: Schematic illustration of the working principle of an analogue-to-digital converter

⇨ Among the A/D converters, the voltage-frequency and delta-sigma (Δ/Σ) converters are the most commonly used systems in testing machines.

D2a. Data processing using the example of a voltage-frequency converter

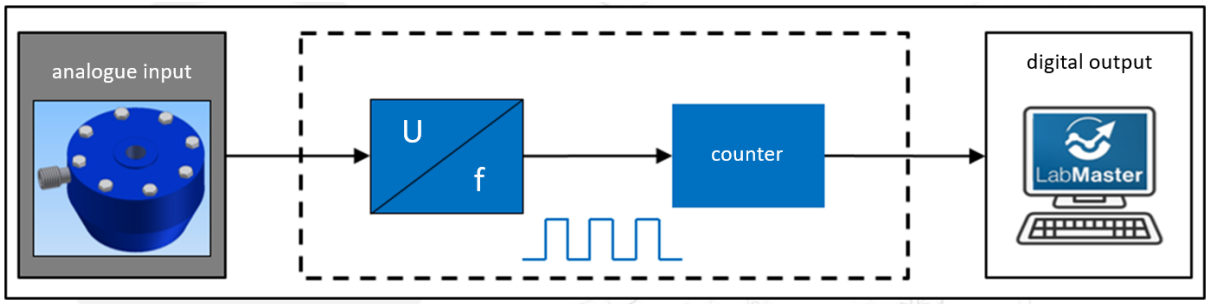


Fig 8: Data processing (input – processing – output) of a voltage-frequency converter

Correlation between resolution/integration time for voltage-frequency converter

The resolution of the voltage-frequency conversion is directly dependent on the duration in which a moving average is calculated from the values recorded by the counter (= **integration time**). The frequency of the averaging thus forms the measurement acquisition rate.

⇨ This means that the **sampling rate is not equal to the data acquisition rate**. A high sampling rate is of no use as long as the measured values cannot be processed accordingly!

A **high resolution** is only achieved with high integration times. However, "fast" processes and events such as peak values or yield points are "smoothed" by the sliding averaging over larger time intervals and thus may not be detected!

→ **For this reason, a high resolution will not necessarily lead to increased accuracy!**

Integration time [ms]	1	10	20	100
Theoretical resolution [digits]	± 9 000	± 90 000	± 180 000	± 900 000
Digit [N] = nominal capacity of load cell / digits	10 000N/9 000 = 1.11 N	10 000N/90 000 = 0.11 N	10 000N/180 000 = 0.055 N	10 000N/900 000 = 0.011 N
Varations of readings [N]	± 1.2	± 0.22	± 0.1	± 0.04

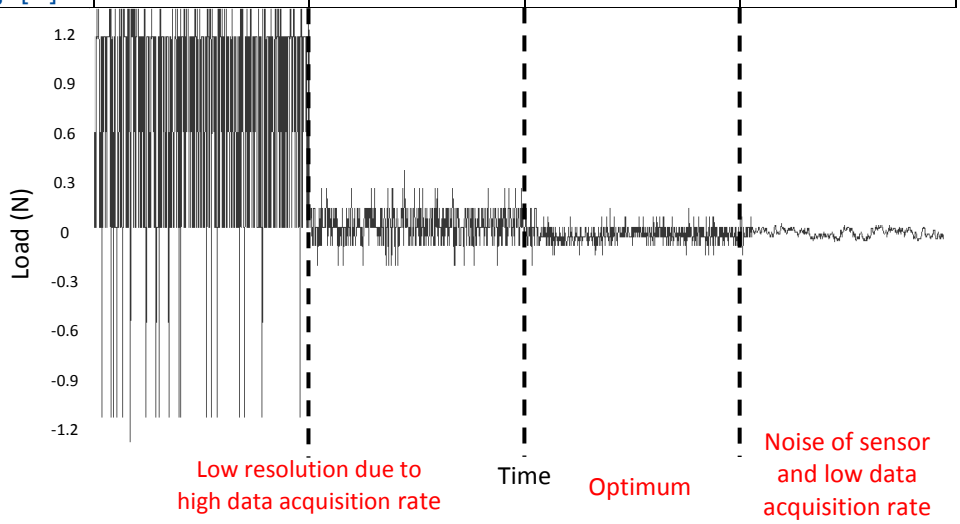
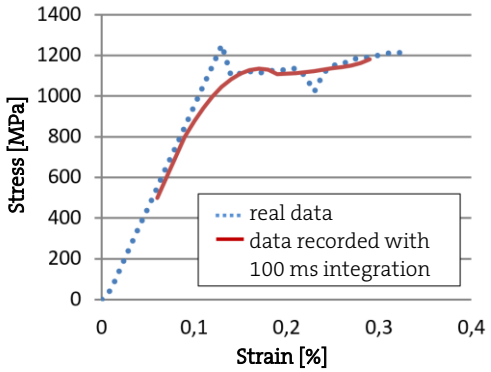


Fig. 9: Resolution at different intergration times using the example of a 10 kN load cell

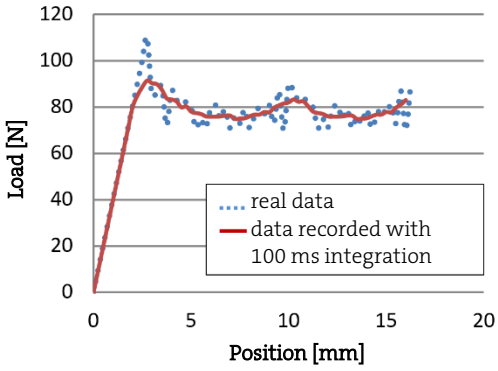
Effects of an excessively high integration time at the voltage-frequency converter using real examples

Determination of the yield strength in the metal tensile test



- force value is a floating average of the force signal within the integration window
- fast stress changes are strongly damped
- correct evaluation of the yield strengths is therefore not possible

Separation & peeling test



- high integration time leads to significant smoothing of the real peak values
- tearing force and other peak values cannot be evaluated and displayed correctly as a result

D2b. Data processing using the example of a delta-sigma (Δ/Σ) converter

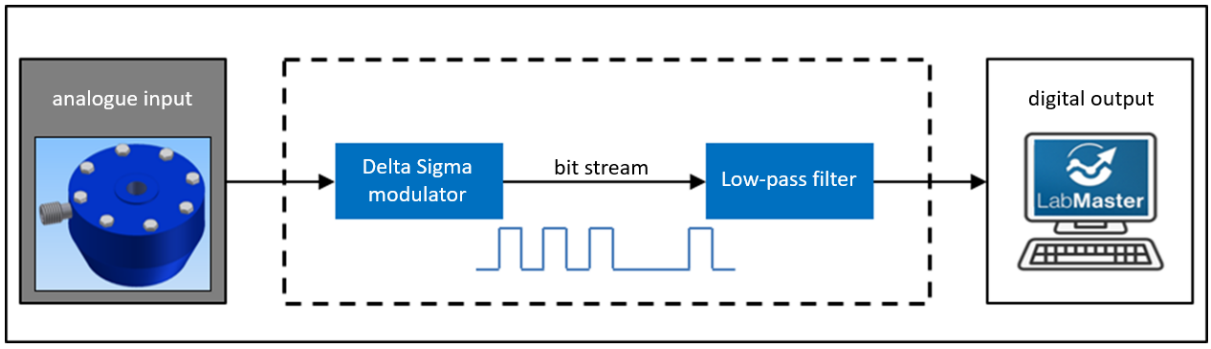


Fig. 10: Data processing (input – processing – output) of a delta-sigma (Δ/Σ) converter

Process of A/D signal conversion using the Δ/Σ -converter

The delta-sigma modulator converts the analogue input signal from the load cell into a bitstream of "0" and "1". Which bit value is taken depends on the incoming analogue value.

A digital 1-bit output signal, similar to the initial analogue signal, is then modulated from the bit stream.

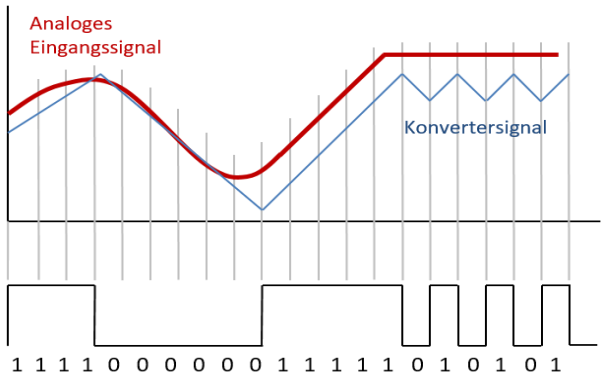


Fig. 11: Schematic illustration of the signal transformation in a Δ/Σ converter

Term	Explanation
Modulator	The modulator generates a bitstream from the analogue signal.
Modulation frequency	Frequency for the modulation within the modulator (in range of MHz)
Bit stream	Produced serial signal consisting of either “0” or “1” Analogue signal rises → Bit value „1“ Analogue signal drops → Bit value „0“ Analogue signal is constant → Bit changes between “0” and “1”
Low pass filter	The low pass filter erases interfering high frequency signals, which occur during signal modulation. As a result, a very high (theoretical) resolution can be achieved.
Measurement acquisition rate	Output frequency of the A/D converter and input frequency of the control (normally 20 kHz)
Oversampling	Oversampling means, that the Output frequency of the A/D converter is higher than control freuqency of the controller (20 for internal processing rate of 1 kHz).

Exemplary signals of Δ/Σ converters, registered on a 10kN load cell

Integration time [ms]	1	10	20	50	100
Measurement acquisition rate [Hz]	1.000	100	50	20	10
Theoretical resolution [digits] 24 bit	±8 388 608	±8 388 608	±8 388 608	±8 388 608	±8 388 608
Digit = nominal load [N] / digits	0.001 N	0.001 N	0.001 N	0.001 N	0.001 N
(true) Resolution [digits]	± 300 000	± 450 000	± 700 000	± 1 000 000	± 1 400 000
Varations of readings [N]	± 0.5	± 0.15	± 0.11	± 0.05	± 0.04

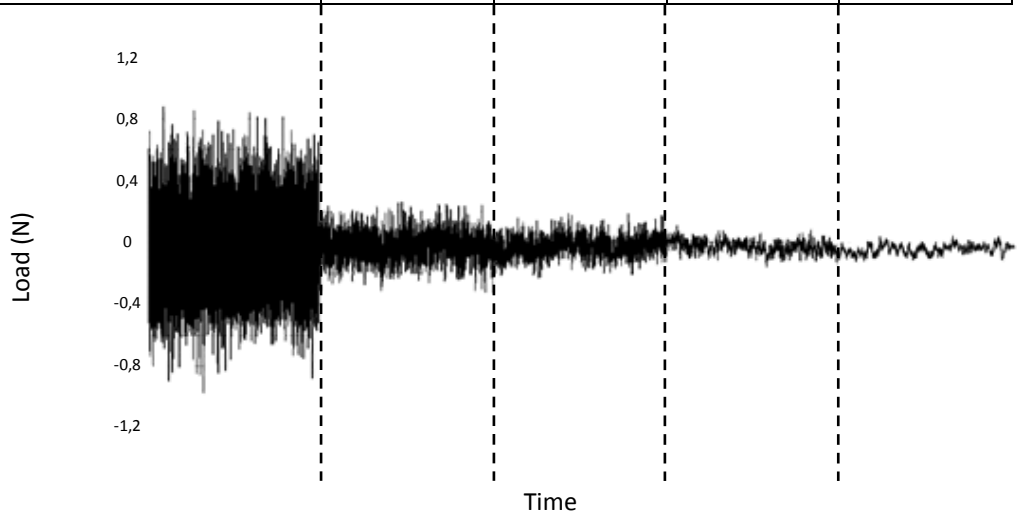


Fig. 12.: Signals of a 10 kN load cell for different integration times/data acquisition rates (see above)

The **nominal resolution** of the Δ/Σ-converter (24 bit independently of integration time) is significantly higher than the one from the voltage-frequency converter (≈17 bit at 20 ms integration time). Anyway, for Δ/Σ-converters the variations of readings are reduced due to background noise. Anyway, with a low pass filter the interfering high frequency noises occurring during modulation can be filtered very well. The analysis of the signals of the load cell reveals that the **variations of readings** of the Δ/Σ-converter are fundamentally higher in comparison to that of the voltage-frequency converter.

⇨ **Variation of readings can be decreased with the Δ/Σ-converters**

There is still some signal noise in the low pass filtered output signal of the Δ/Σ-converter. The amplitude of this noise depends on oversampling rate and order of the Δ/Σ-modulator

⇨ **Background noise can be reduced by:**
... high sampling rates / high oversampling
... high order Δ/Σ-modulators

A **too high integration** time leads to averaging and impermissible smoothing of recorded characteristic material properties like Yield strength and other peak values. This is true for both A/D converters!
Therefore, the right choice of integration time is elementary for an optimal ratio of true resolution and data acquisition rate.